**DAILY ASSESSMENT FORMAT**

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| **Date:** | **04-06-2020** | **Name:** | **HEMALATHA SANIL** |
| **Course:** | **Digital Design using HDL** | **USN:** | **4AL17EC035** |
| **Topic:** | **1.Hardware modelling using Verilog**  **2.FPGA and ASIC Interview Questions.** | **Semester & Section:** | **6 SEM & ‘A’ SEC** |
| **Github Repository:** | **Hemalatha-Sanil** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**          **Task 4: Implement a simple T-FlipFlop and test the module using a compiler**      **Youtube live session on ELECTRICAL ENGINEERING by Prof.Anirudhdhan,IIT Madras**  **(03-06-2020)** |

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| **Date:** | **04-06-2020** | **Name:** | **HEMALATHA SANIL** |
| **Course:** | **PYTHON** | **USN:** | **4AL17EC035** |
| **Topic:** | **Section 31** | **Semester & Section:** | **6 SEM & ‘A’ SEC** |
| **Github Repository:** | **Hemalatha-Sanil** |  |  |

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| **AFTERNOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**    **APPLICATION 9: Build a web-based Financial Graph** |

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